

Customer No.: 31561  
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In The Abstract

A pipeline accessing method to a large block memory is described. The large block flash memory has a plurality of pages and each page has a plurality of sectors~~[[by N]]~~. The memory device has a controller to control an access operation between a host and a cell array of the large block flash memory with a page buffer. The controller includes at least two buffers, when the host intends to program the memory device. In the method, data sectors are transferred between the host and the large block flash memory by alternatively using the buffers. After transferring N data sectors with respect to one page, a start program command is issued by the controller for programming the data.